Approved in 39th BoA Meeting (25-03-2021)

Course Number: EE560
Course Name: Reconfigurable Computing
Credits: 3-0-2-4
Prerequisites: EE 210/201P- Digital System Design & Practicum, CS 201/201P- Computer Organization & Practicum.
Intended for: PG/UG
Distribution: Elective for M. Tech (VLSI), UG and other PG courses

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1. Preamble: Application level parallelism in the new age computer architecture is gaining much attention with the recent achievements in the VLSI technology. Reconfigurable computers offer the advantage of configuring hardware and programming the interconnections as per the application in comparison to the fixed hardware elements (and interconnections) in a general purpose microprocessor. The aim of this course is to investigate the state-of-the-art in reconfigurable computing and motivating hardware-software co-design on FPGA. The concepts of reconfigurable computing will be validated with experiments on various numerical, signal processing and cryptographic algorithms.

2. Course Modules with Quantitative Lecture Hours: This course has three hour lecture session accompanied by two hours of laboratory session per week. List of course modules are provided below.

1. **Introduction to reconfigurable computing :** **[3 Hours]**
   Reconfigurable computing, history and survey, fixed Vs reconfigurable computing, applications of reconfigurable computing
2. **FPGA Design** : **[6 Hours]**
   Introduction to FPGA, LUT devices and mapping, partitioning, placement and routing algorithms. A case study on ALU design
3. **Reconfigurable computing architectures:** **[5 Hours]**
   Performance evaluation, Coarse grained and fine grained reconfigurable computing, a case study on coarse grained reconfigurable computing, Multi-FPGA architectures, Dynamic reconfiguration, total versus partial reconfiguration
4. **Reconfigurable computing :** **[2 Hours]**
   Power Reduction techniques for FPGA
5. **Reconfigurable computing applications** **[6 Hours]**
   Distributed Arithmetic, CORDIC algorithm on FPGA
6. **Reconfigurable computing – Security to FPGA** **[4 Hours]**
   Physical Unclonable Functions-Introduction and implementation on FPGA, on-chip authentication of FPGA-based devices
7. **Hardware-Software Co-design** **[4 Hours]**
   Introduction, Partitioning, Scheduling, Synthesis, Retiming, Pipelining. Unfolding, analysis and Estimation
8. **Finite State Machine with Datapath** **[3 Hours]**
   Introduction, finite state machines, finite state machine with datapath (FSMD), a case study on FSMD
9. **Hardware –Software Interfaces** **[3 Hours]**

Hardware software Communication, one way and two way handshake, blocking and non-blocking data transfer, On-chip Bus, Bus transfer and topologies

10. Case study **[6 Hours]**

Decoders, Crypto processor, CORDIC processor.

Experiments: The practicum of this course implements the FPGA based implementation of the algorithms and architectures discussed during the course. Experiments such as UART interfacing with FPGA, CORDIC algorithm, interfacing camera with FPGA, image compression and cryptographic algorithm on FPGA.

3. Textbooks:

1. Scott Hauck André DeHon, Reconfigurable Computing, The theory and practice of FPGA based Computation, 1st edition, Morgan Kaufmann, 2008.
2. F. Vahid and T. Givargis, "Embedded Systems: A Unified Hardware Software Introduction", John Wiley and Sons, 2011.

4. **References:**

1. Patrick Schaumont, "A Practical Introduction to Hardware/Software Co design", Springer, 2010, ISBN 978-1-4614-3736-9 and ISBN 978-1-4614-3737-6.
2. **Bobda**, Christophe, Introduction to Reconfigurable Computing: Architectures, algorithms and applications, Springer, 2007.
3. I. Koren, "Computer Arithmetic Algorithms". A.K. Peters Ltd., 2002.
4. Behrooz Parhami, "Computer Arithmetic- Algorithms and Hardware Designs", Oxford university press, 2nd Edition. 2010.
5. Peter J. Ashenden, "The designer's guide top VHDL", Morgan Kaufmann, 2008.
6. IEEE research papers on relevant topics.

Similarity Content Declaration with Existing Courses:

S.No	Course Code	Similarity content	Approximate %
1.	EE 529	Introduction to FPGA, Hardware Software co-design	< 20 %
2.	EE208P	Introduction to FPGA	< 5 %
3.	EE 523	CORDIC Based Architecture	< 10 %

Justification for new course proposal if cumulative similarity content is >30%: N/A